**ACADEMIC PLANNER**

**B.Sc.(H) I Sem**

**Computer System Architecture**

**Teacher: Dr. Shalini Sharma**

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| **CHAPTERS** | **UNIT** | **COMPLETION MONTH** | **ASSESSMENT** |
| Ch 1: Digital Logic Circuits | UNIT 1 | August |  |
| Ch 2: Digital Components | UNIT 2 | September | * Test unit1 * Assignment Ch1 &Ch2 * Problem Solving exercise in class |
| Ch 4: Register Transfer and Micro-operations |
| Ch 3: Data Representation | UNIT 3 | September |
| Ch 5: Basic Computer Organization and Design | UNIT 4 | October | * Test unit 2 + unit 3 * Presentation unit 1,2 &3 * Quiz unit 4 |
| Ch 9: Pipeline and Vector Processing |
| Ch 8: Central Processing Unit | UNIT 5 | October | * Test unit 4 & unit 5 * Problem solving assignments * Presentation unit 4 & unit 5 |
| Ch-7: Multicores, Multiprocessors, and Clusters | November |
| Ch 11: Input Output Organization | UNIT 6 | November | * Test unit 6 * Mock practical & viva * Presentation unit 6 |
| Ch 12: Memory Organization |